ABSTRACT OF THE DISCLOSURE

A semiconductor memory device capable of enhancing a production yield is provided. A dummy control circuit activates a first dummy column including a plurality of dummy cells placed at a position close to a row decoder in a row direction and a second dummy column including a plurality of dummy cells placed at a position farthest from the row decoder in a row direction with a plurality of memory cells interposed between the first dummy column and the second dummy column, through first and second dummy word lines. A dummy column selector selects either one of a signal on a first dummy bit line connected to the first dummy column and a signal on a second dummy bit line connected to the second dummy column, and outputs the selected signal to an amplifier control circuit. The amplifier control circuit generates an amplifier startup signal with respect to an amplifier circuit based on a signal from the dummy column selector.